WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate in which a source, drain and channel are formed;

a gate formed on a gate dielectric layer formed on the semiconductor substrate;

spacers adjacent to the gate wherein the gate and spacers are formed in a trench formed in a layer of dielectric material formed on the substrate surface.

2. The semiconductor device of claim 1 wherein the distance between the spacers defines a device gate length.

3. The semiconductor device of claim 2 wherein the distance between the spacers is less than 50 nm.

4. A process for device fabrication comprising:

forming a sacrificial gate over an active region of a semiconductor substrate wherein the width of the sacrificial gate is selected to define the distance between a source region and a drain region in the semiconductor substrate;

forming a trench dielectric layer adjacent to the sacrificial gate;

removing the sacrificial gate, thereby defining a trench in the trench dielectric layer;

forming spacers in the trench; and

forming a device gate in which at least a portion of the gate is formed between the spacers.

5. The process of claim 4 wherein a first layer of dielectric material is formed on the semiconductor substrate before the sacrificial gate is formed thereon and wherein the sacrificial gate is formed on the active region of the substrate.

6. The process of claim 5 wherein the active region in the semiconductor substrate is defined by shallow trench isolation.

7. The process of claim 6 further comprising implanting dopant into the semiconductor substrate after the sacrificial gate is formed thereover, wherein the implant conditions are selected to define a source and a drain region in the semiconductor substrate.

8. The process of claim 6 further comprising implanting dopant into the semiconductor substrate after the spacers are formed thereover.

9. The process of claim 6 wherein the gate is formed by:

forming a gate dielectric layer between the spacers;

forming a gate electrode over the gate dielectric layer;

forming a layer of metal over the gate electrode; and

patterning the layer of dielectric material with the layer of metal thereover to form the gate.

10. The process of claim 4 wherein the trench dielectric layer is formed by:

depositing a layer of trench dielectric material over the substrate with the sacrificial gate thereon;

polishing the layer of trench dielectric material; and

stopping the polishing of the trench dielectric material after the sacrificial gate is exposed therethrough.

11. The process of claim 10 wherein the trench dielectric layer is a layer of silicon dioxide and the sacrificial gate is silicon nitride.

12. The process of claim 11 wherein the trench dielectric layer is deposited from a high density plasma.

13. The process of claim 11 wherein the sacrificial gate is removed using a wet etch.

14. The process of claim 11 wherein the spacers are silicon nitride.

15. The process of claim 11 wherein the spacers are formed by:

depositing a layer of silicon nitride on the surface of the semiconductor substrate with the trench dielectric layer thereon after the trench is formed in the trench dielectric layer; and

anisotropically etching the silicon nitride layer to form the spacers.

16. The process of claim 15 further comprising a local channel implant after the spacers are formed.

17. The process of claim 15 further comprising a local channel implant after the trench is formed.

18. The process of claim 15 further comprising removing the oxide from a portion of the semiconductor substrate surface between the spacers.

19. The process of claim 9 wherein the gate dielectric layer is selected from the group consisting of silicon dioxide, silicon oxynitride and tantalum oxide.

20. The process of claim 9 wherein the gate electrode is doped polycrystalline silicon.